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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,686	LEMPEL, ODED	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 have been considered. Claims 6-9, 13, 16, 27, and 28 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received 16 June 2006.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 4-5, 7-8, 10-14, 16-20, 23-24, and 26 are rejected under 35 U.S.C. 102(b) as being taught by Schroter, U.S. Patent Number 6,338,133 (herein referred to as Schroter).

5. Referring to claim 1, Schroter has taught apparatus comprising:

a. A branch prediction unit to predict whether a branch is to be taken (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2);

b. An instruction fetch unit to fetch an instruction (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2); and

c. A control circuit coupled to the branch prediction unit, wherein the control circuit is to abort the fetched instruction at a pre-decoding stage if the branch is predicted to be taken (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2).

6. Referring to claim 4, Schroter has taught wherein the instruction fetch unit is to fetch a branch target if the branch prediction unit determines that the branch is predicted to be taken (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2).

7. Referring to claim 5, Schroter has taught wherein the branch prediction unit is to transmit a branch taken signal to the control circuit if the branch is predicted to be taken (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2).

8. Referring to claim 7, Schroter has taught wherein the fetched instruction is a next sequential (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2).

9. Referring to claim 8, Schroter has taught a method comprising:

a. Predicting whether a branch is to be taken (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2);

b. Fetching a next instruction (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2);

c. Terminating a process associated with the next instruction if the branch is predicted to be taken (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2).

10. Referring to claim 10, Schroter has taught redirecting an instruction fetch unit to the predicted branch if the branch is predicted to be taken (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2).

11. Referring to claim 11, Schroter has taught fetching a branch target by the instruction fetch unit if the branch is predicted to be taken (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2).

12. Referring to claim 12, Schroter has taught transmitting a branch taken signal to a control circuit if the branch is predicted to be taken (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2).

13. Referring to claim 13, Schroter has taught terminating power for processes associated with the next instruction if the branch signal is received (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2).

14. Referring to claim 14, Schroter has taught an apparatus comprising:

a. Means for predicting whether a branch is to be taken (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2);

b. Means for fetching a next sequential instruction (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2); and

c. Means coupled to the branch prediction unit for aborting the next sequential instruction if the branch is predicted to be taken (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2).

15. Referring to claim 16, Schroter has taught a system comprising:

a. A bus (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2);

b. An external memory coupled to the bus (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2); and

c. A processor coupled to the bus (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2), the processor including:

i. A branch prediction unit to predict whether a branch is to be taken (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2);

ii. A instruction fetch unit to fetch a next sequential instruction (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2); and

iii. A control circuit coupled to the branch prediction unit, the control circuit to abort the next instruction if the branch is predicted to be taken (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2).

16. Referring to claims 17 and 18, Schroter has taught wherein the bus is a PCI bus or an ISA bus (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2). In regards to Schroter, Schroter has taught there are busses present, which includes PCI and ISA busses.

17. Referring to claims 19 and 20, Schroter has taught wherein the external memory is a SRAM or a DRAM (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2). In regards to Schroter, Schroter has taught that the external memory is a random access memory, which includes both SRAM and DRAM.

18. Referring to claim 23, Schroter has taught wherein the instruction fetch unit is to fetch a branch target if the branch prediction unit determines that the branch is predicted to be taken (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2).

19. Referring to claim 24, Schroter has taught wherein the branch prediction unit is to transmit a branch taken signal to the control circuit if the branch is predicted to be taken (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2).

20. Referring to claim 26, Schroter has taught wherein the next instruction is a next sequential instruction (Schroter column 1, lines 26-53; column 4, lines 11-44; Figure 1; and Figure 2).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 2-3, 6, 9, 15, 21-22, 25, 27, and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schroter, U.S. Patent Number 6,338,133 (herein referred to as Schroter) in view of Thusoo et al., U.S. Patent Number 5,809,272 (herein referred to as Thusoo).

23. Referring to claims 2, 3, 6, 9, 15, 21, 22, and 25, Schroter has taught

a. An instruction decoder, wherein the control circuit is to block data associated with the instruction from entering the instruction decoder (Applicant's claims 2 and 21) (Schroter column 1, lines 27-53; column 4, lines 11-44; Figure 1; and Figure 2).

b. An instruction decoder, wherein the control circuit is to block processing of data associated with the instruction by the instruction decoder (Applicant's claims 3 and 22) (Schroter column 1, lines 27-53; column 4, lines 11-44; Figure 1; and Figure 2).

c. Wherein the control circuit is to prevent an output of a cache array to be input to an instruction decoder in response to the branch taken signal (Applicant's claims 6 and 25) (Schroter column 1, lines 27-53; column 4, lines 11-44; Figure 1; and Figure 2).

d. Blocking data associated with the next instruction from entering an instruction length decoder if the branch is predicted to be taken (Applicant's claim 9) (Schroter column 1, lines 27-53; column 4, lines 11-44; Figure 1; and Figure 2).

e. Means for preventing information associated with the next sequential instruction from being sent to an instruction decoder if the branch is predicted to be taken (Applicant's claim 15) (Schroter column 1, lines 27-53; column 4, lines 11-44; Figure 1; and Figure 2).

24. Schroter has not taught an instruction length decoder. However, Schroter has taught a superscalar system capable of executing instructions in general (Schroter column 1, lines 16-26). Thusoo has explicitly taught a superscalar device that executes CISC, i.e. variable length, instructions and the instruction length decoders to decode CISC instructions (Thusoo column 1, line 44 to column 2, line 13; column 4, line 49 to column 5, line 4; and Figure 2). In regards to Schroter in view of Thusoo, Schroter has taught that pre-fetched instructions, e.g. instructions that have been fetched to the sequential queue but not yet decoded, sequentially following a branch instruction are halted, e.g. aborted and blocked from continued execution, when the branch is predicted taken and Thusoo has taught that length decoding is done in the decoding stage, so the data associated with the aborted instruction is blocked from ever reaching the decoder. A person of ordinary skill in the art at the time the invention was made would have

recognized that the instruction length decoder allows for a higher compatibility in the device, since a variable instruction set can now be run on the device, and, as taught by Thusoo, the variable length instruction decoders reduce delay for decoding variable length instructions and reduce complexity and cost (Thusoo column 2, lines 5-13 and column 4, line 49 to column 5, line 4). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the instruction length decoders of Thusoo in the device of Schroter to increase program instruction compatibility and reduce delay, complexity, and cost.

25. Referring to claim 27, Schroter has taught apparatus comprising:

a. An instruction pointer to fetch a next sequential instruction for processing (Schroter column 1, lines 27-53; column 4, lines 11-44; Figure 1; and Figure 2);

b. An instruction cache array coupled to the instruction pointer to output information associated with the next sequential instruction (Schroter column 1, lines 27-53; column 4, lines 11-44; Figure 1; and Figure 2);

c. A latch coupled between the output of the instruction cache array and a instruction decoder (Schroter column 1, lines 27-53; column 4, lines 11-44; column 5, lines 50-61; Figure 1; and Figure 2). In regards to Schroter, a register is a latch. Please see Heuring and Jordan's Computer Systems Design and Architecture ©1997 pages 151.

d. A circuit to open the latch to prevent the information associated with the next sequential instruction from being output if a branch taken signal is received, wherein the branch taken signal indicates that a branch has been predicted to be

taken (Schroter column 1, lines 27-53; column 4, lines 11-44; Figure 1; and Figure 2).

26. Schroter has not taught an instruction length decoder. However, Schroter has taught a superscalar system capable of executing instructions in general (Schroter column 1, lines 16-26). Thusoo has explicitly taught a superscalar device that executes CISC, i.e. variable length, instructions and the instruction length decoders to decode CISC instructions (Thusoo column 1, line 44 to column 2, line 13; column 4, line 49 to column 5, line 4; and Figure 2). In regards to Schroter in view of Thusoo, Schroter has taught that pre-fetched instructions, e.g. instructions that have been fetched to the sequential queue but not yet decoded, sequentially following a branch instruction are halted, e.g. aborted and blocked from continued execution, when the branch is predicted taken and Thusoo has taught that length decoding is done in the decoding stage, so the data associated with the aborted instruction is blocked from ever reaching the decoder. A person of ordinary skill in the art at the time the invention was made would have recognized that the instruction length decoder allows for a higher compatibility in the device, since a variable instruction set can now be run on the device, and, as taught by Thusoo, the variable length instruction decoders reduce delay for decoding variable length instructions and reduce complexity and cost (Thusoo column 2, lines 5-13 and column 4, line 49 to column 5, line 4). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the instruction length decoders of Thusoo in the device of Schroter to increase program instruction compatibility and reduce delay, complexity, and cost.

27. Referring to claim 29, Schroter has taught an apparatus comprising:

a. An instruction pointer to fetch a next sequential instruction for processing (Schroter column 1, lines 27-53; column 4, lines 11-44; Figure 1; and Figure 2);

b. A branch prediction unit to determine that a branch is to be taken and generate a branch taken signal (Schroter column 1, lines 27-53; column 4, lines 11-44; Figure 1; and Figure 2);

c. A cache logic array coupled to the instruction pointer to receive data associated with the next sequential instruction and to receive the branch taken signal (Schroter column 1, lines 27-53; column 4, lines 11-44; Figure 1; and Figure 2);

d. An instruction decoder coupled to the cache logic array, wherein responsive to the received branch taken signal, the cache logic array is to abort further processing of the data associated with the next sequential instruction (Schroter column 1, lines 27-53; column 4, lines 11-44; Figure 1; and Figure 2).

28. Schroter has not taught an instruction length decoder. However, Schroter has taught a superscalar system capable of executing instructions in general (Schroter column 1, lines 16-26). Thusoo has explicitly taught a superscalar device that executes CISC, i.e. variable length, instructions and the instruction length decoders to decode CISC instructions (Thusoo column 1, line 44 to column 2, line 13; column 4, line 49 to column 5, line 4; and Figure 2). In regards to Schroter in view of Thusoo, Schroter has taught that pre-fetched instructions, e.g. instructions that have been fetched to the sequential queue but not yet decoded, sequentially following a branch instruction are halted, e.g. aborted and blocked from continued execution, when the branch is predicted taken and Thusoo has taught that length decoding is done in the decoding stage, so the data associated with the aborted instruction is blocked from ever reaching the

decoder. A person of ordinary skill in the art at the time the invention was made would have recognized that the instruction length decoder allows for a higher compatibility in the device, since a variable instruction set can now be run on the device, and, as taught by Thusoo, the variable length instruction decoders reduce delay for decoding variable length instructions and reduce complexity and cost (Thusoo column 2, lines 5-13 and column 4, line 49 to column 5, line 4). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the instruction length decoders of Thusoo in the device of Schroter to increase program instruction compatibility and reduce delay, complexity, and cost.

29. Referring to claim 30, Schroter in view of Thusoo has taught circuitry to block the data associated with the next sequential instruction from entering the instruction length decoder (Thusoo column 1, line 44 to column 2, line 13; column 4, line 49 to column 5, line 4; and Figure 2) if the branch taken signal is received (Schroter column 1, lines 27-53; column 4, lines 11-44; Figure 1; and Figure 2).

30. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schroter, U.S. Patent Number 6,338,133 (herein referred to as Schroter) in view of Thusoo et al., U.S. Patent Number 5,809,272 (herein referred to as Thusoo) as applied to claim 27 above, and further in view of Heuring and Jordan's Computer Systems Design and Architecture ©1997 (herein referred to as Heuring). Schroter in view of Thusoo has not taught an AND gate having a first input, second input and an output, wherein the first input is an inverted branch taken signal and the second input is an inverted clock and the output is used to open the latch. Heuring has taught AND gates controlling whether a latch is open or closed (Heuring pages 71-75). A person of ordinary skill in the art at the time the invention was made, and as taught by Heuring, would

have recognized that AND gates are an important part of supporting and controlling transmission and storage elements (Heuring page 71). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the AND gate of Heuring in the device of Schroter in view of Thusoo to properly control and support transmission and storage elements.

Response to Arguments

31. Examiner withdraws the objections to claims 5 and 24 in view of the persuasive arguments.

32. Examiner withdraws the objection to claim 26 in view of the amended claim.

33. Examiner withdraws the objection to claim 7 in view of the amended claim.

34. Examiner withdraws the 35 USC §112 rejections to claims 6, 8, 25, and 26 in view of the amended claims.

35. Applicant's arguments filed 16 June 2006 have been fully considered but they are not persuasive. Applicant's argue in essence on pages 8-11

> ...Here, in contrast, the invention...unambiguously indicates that it aborts the fetched instructions prior to the resolution of the branch. Accordingly, *Schroter* fails to anticipate every element...and the Applicant respectfully requests withdrawal of the...rejection...

36. This has not been found persuasive. *Schroter* teaches further in the paragraph recited in the arguments that branch prediction is utilized to predict the outcome of a branch and that the next sequential instruction is halted, e.g. aborted, for the speculative target instruction (Schroter column 1, lines 37-50). *Schroter* further teaches the use of branch prediction in the device

described in column 4, lines 11-44 and shows it in Figure 1 and Figure 2. Therefore, *Schroter* has taught that the invention aborts the fetched instruction, e.g. the next sequential instruction is halted, in favor of the speculative, e.g. unknown and unresolved, target instruction. This means that the next sequential instruction is aborted before the branch instruction has been resolved.

Conclusion

37. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

38. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

40. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

41. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
6 September 2006

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